

**VARIABLE SPEED DRIVES  
HARMONIC EFFECTS**

**&**

**EFFECT OF USE WITH LONG CABLES (100 – 300m)**

**ZEST**

**Electric Motors & Drives**

*....OUR VISION, YOUR SOLUTION .....*

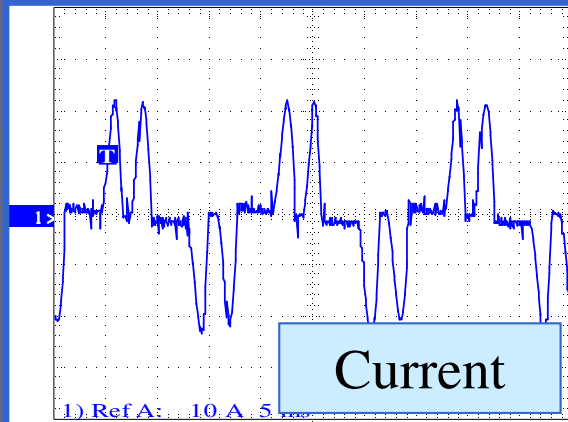
*TOGETHER WE DRIVE THE  
FUTURE!*



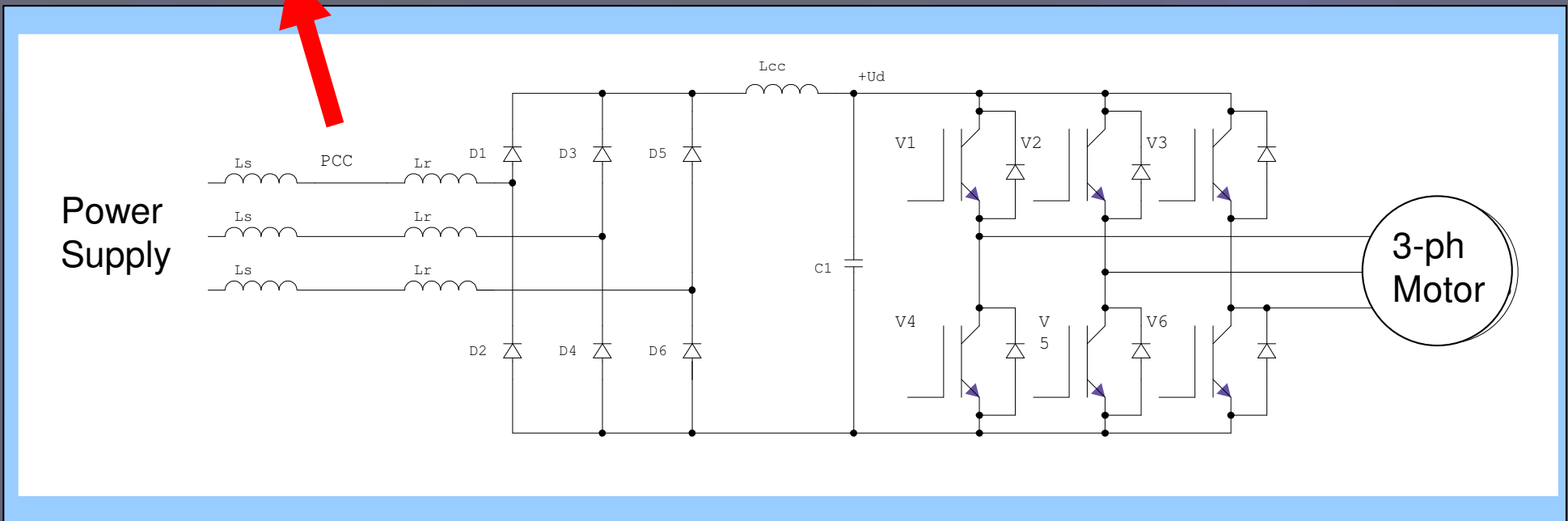
# HARMONIC EFFECTS



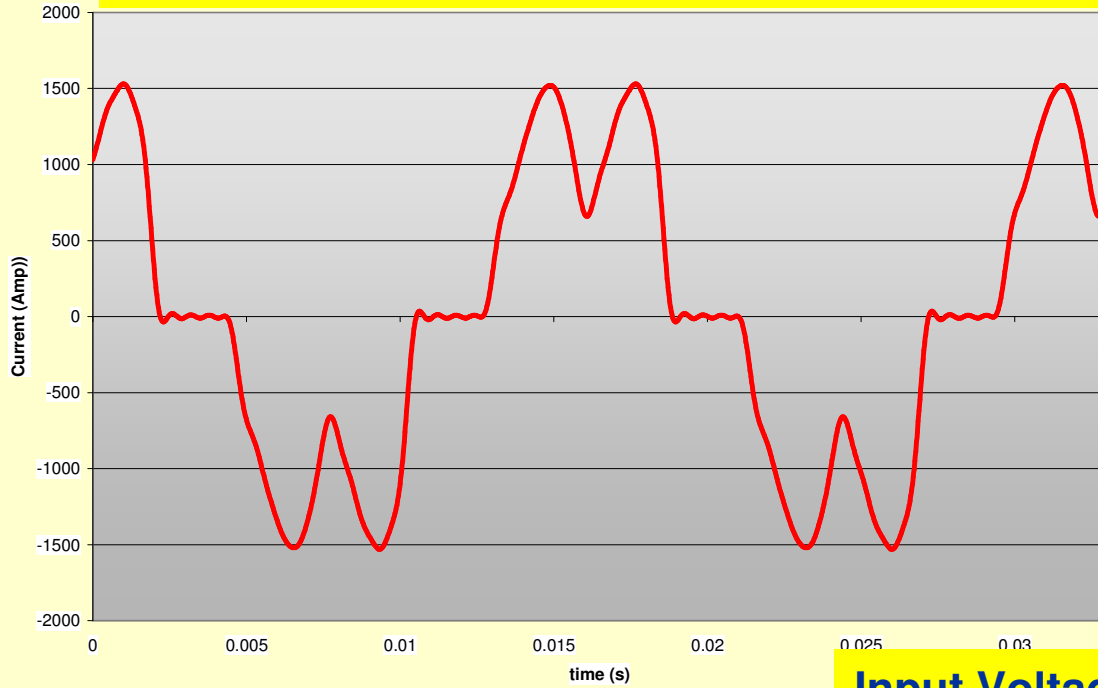
# VSD Typical Input current wave form



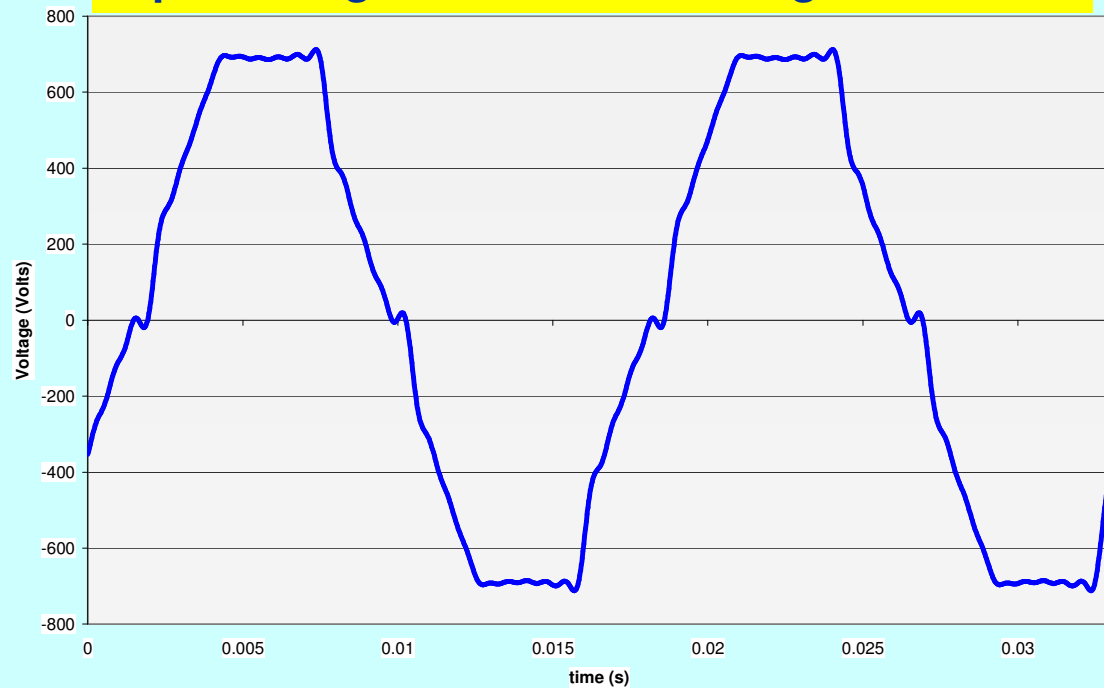
**N.B. This effect is common and similar to all Voltage Source PWM VSDs**



## Input Current distortion resulting from a VSD



## Input Voltage distortion resulting from a VSD

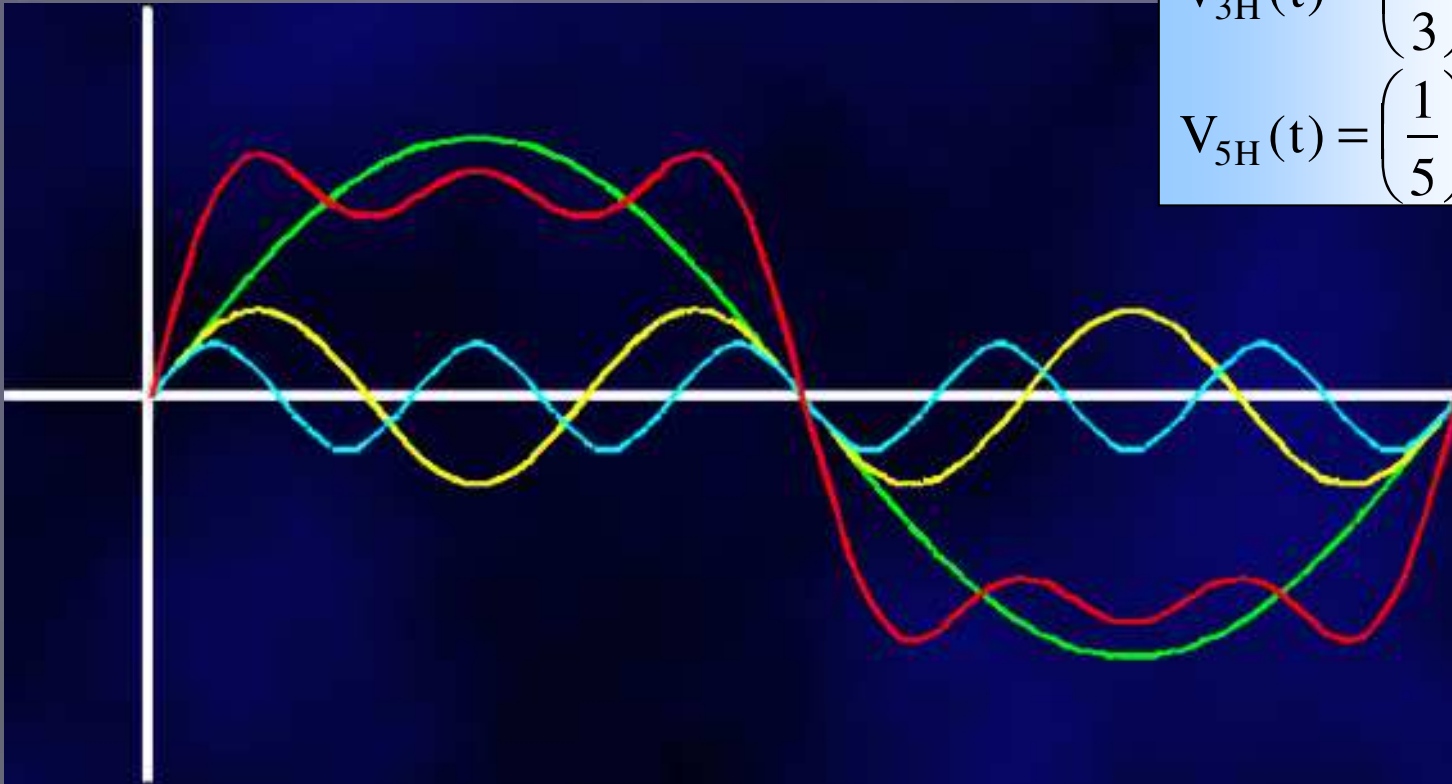




$$V(t) = \sqrt{2} \cdot V_{rms} \cdot \sin(\omega \cdot t) \quad +$$

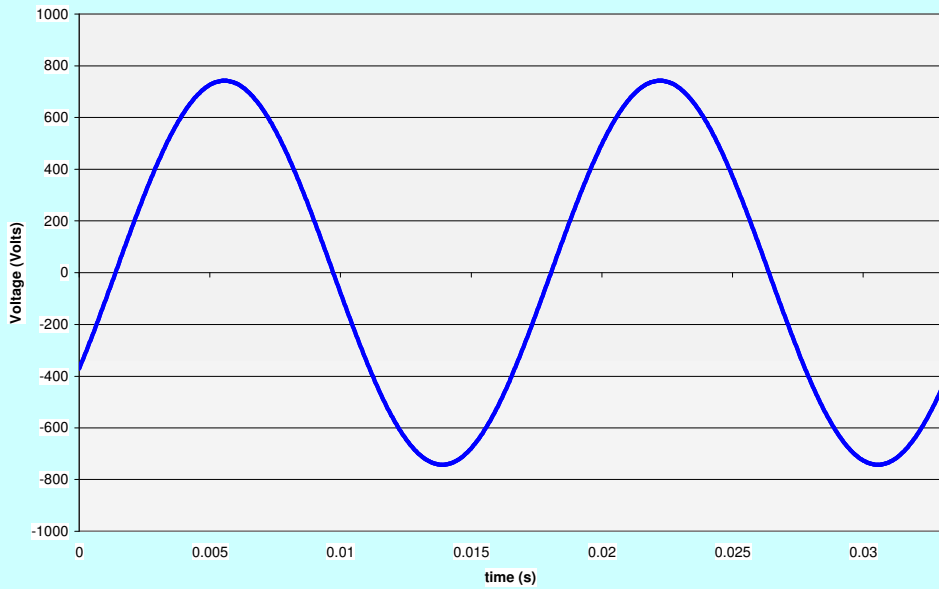
$$V_{3H}(t) = \left(\frac{1}{3}\right) \cdot \sqrt{2} \cdot V_{rms} \cdot \sin(3 \cdot \omega \cdot t) \quad +$$

$$V_{5H}(t) = \left(\frac{1}{5}\right) \cdot \sqrt{2} \cdot V_{rms} \cdot \sin(5 \cdot \omega \cdot t)$$

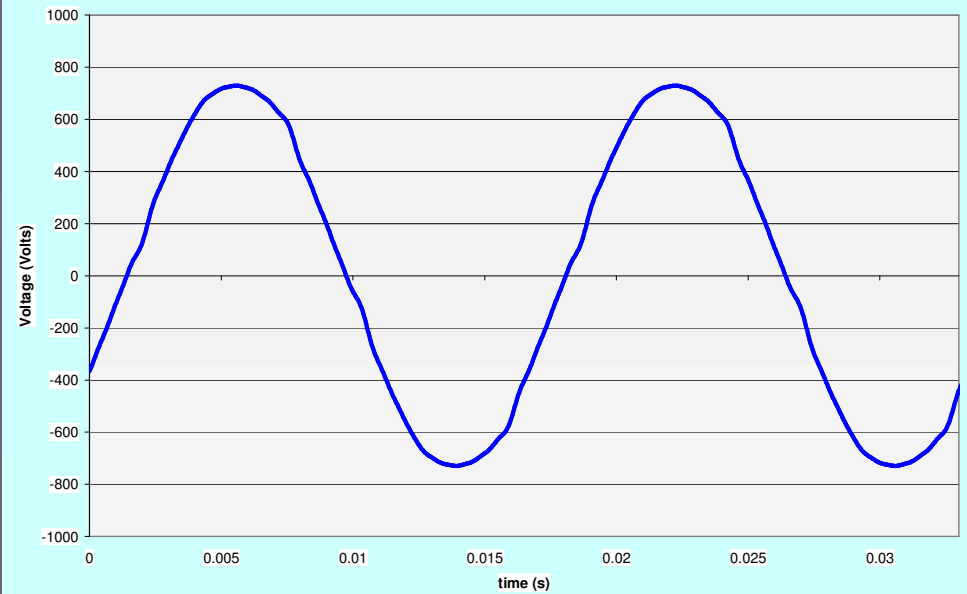


$$V_{tot}(t) = \sqrt{2} \cdot V_{rms} \cdot \left[ \sin(\omega \cdot t) + \frac{1}{3} \cdot \sin(3 \cdot \omega \cdot t) + \frac{1}{5} \cdot \sin(5 \cdot \omega \cdot t) + \frac{1}{7} \cdot \sin(7 \cdot \omega \cdot t) + \dots \right]$$

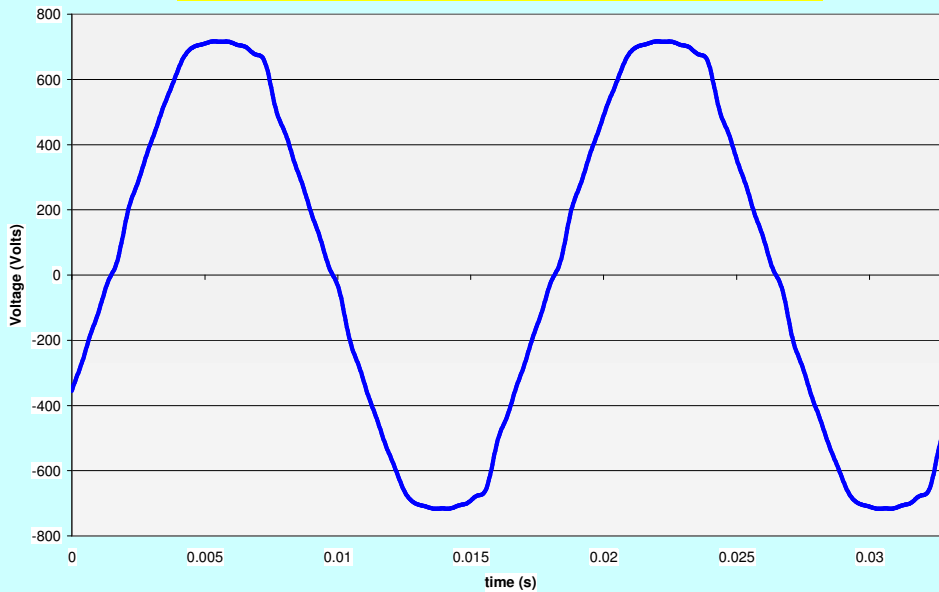
**Input sine wave 0% THD**



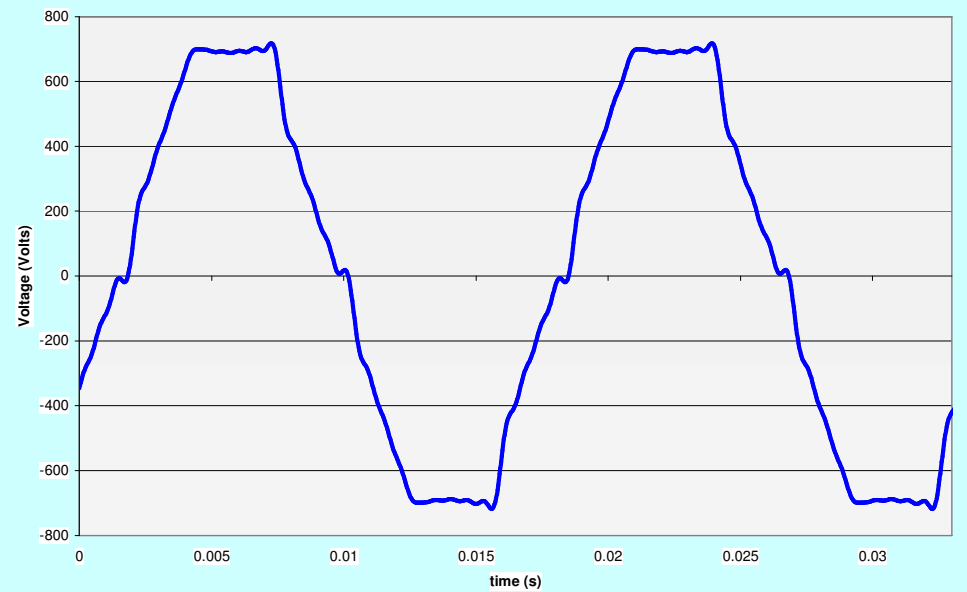
**Input sine wave 4% reactor, 2.4% THD**



**Input sine wave 1% reactor, 3.6% THD**



**Input sine wave 8% THD**





# HARMONICS – POSSIBLE SOLUTIONS

1. Use an AC line reactor
2. VSD design with built in DC choke
3. Install harmonic filters
4. Use 12 pulse VSD
5. Use regenerative / active front end VSD design



# HARMONICS – POSSIBLE SOLUTIONS SUMMARY

VSD Type	Typical I THD	Cost
Standard 6 pulse	101%	100%
6 pulse with 2% reactor	56%	103%
6 pulse with 4% reactor	39%	105%
12 pulse	12%	200%
Regenerative	3%	250%





## **HARMONICS – THE WEG SOLUTION:**

- 1. All 525V WEG VSDs >32A have a built in DC choke.**
- 2. In all other cases, or for greater harmonic reduction use a line reactor of 2 – 4% rating. In most installations this is an acceptable solution.**
- 3. For high power  $\geq 500\text{kW}$  applications consider a 12 pulse VSD or active front end design if harmonics levels are a cause of concern.**



## INPUT REACTORS – WHAT IS IMPORTANT TO REMEMBER:

1. The harmonic values for all reputable AC VSDs are **very similar**.
2. The Voltage harmonic distortion value is affected by the customer supply transformer rating and electrical network – We cannot give a value without knowing his system detail
3. Built in AC reactors have little technical value – it's mostly a marketing exercise
4. Built in DC chokes have technical value
  1. Give a similar result to a 2% AC line reactor
  2. Do not cause a volt drop ( as an AC reactor does )
  3. ***All the WEG 525V VSDs >32A have a built in DC choke***
5. Input reactors are also useful to reduce the effect of dips, sags, swells, transients and other line side disturbances

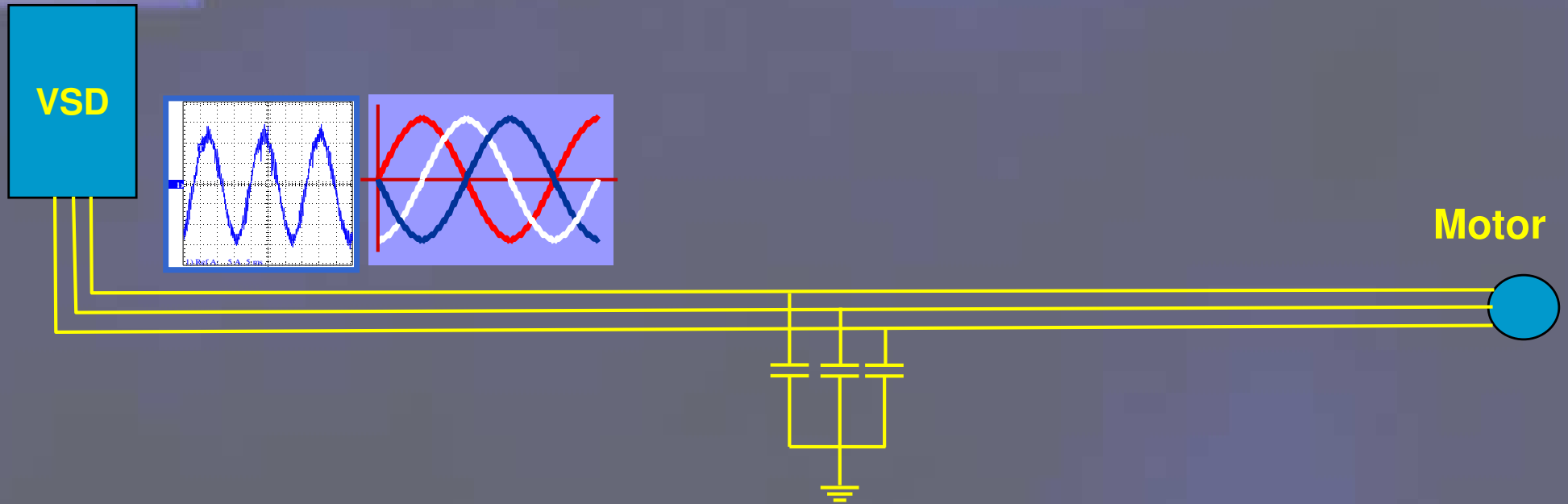


## **MAIN PROBLEMS ASSOCIATED WITH LONG CABLES BETWEEN VSD AND MOTOR**

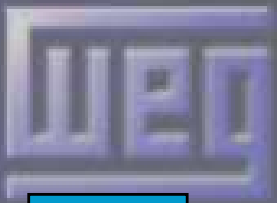
- 1. Capacitive leakage current**
- 2. Voltage reflections causing high  $V_{peak}$  and  $dv/dt$  values**



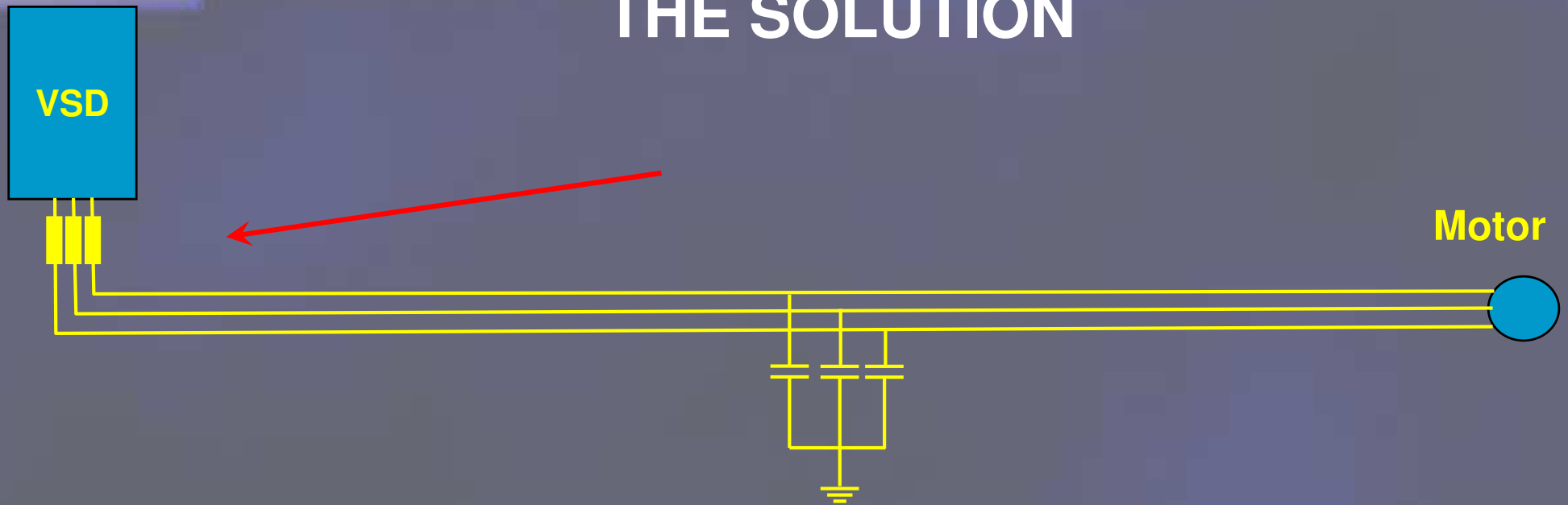
# CAPACITIVE LEAKAGE CURRENTS



1. The VSD output is not a pure and balanced sinusoidal waveform as supplied by Eskom
2. On long cables the cable conductor and insulator properties combine to behave like a capacitor
3. The combination causes capacitive leakage current of significant values in cables  $> 100\text{m}$
4. *This effect is common to all PWM VSDs*



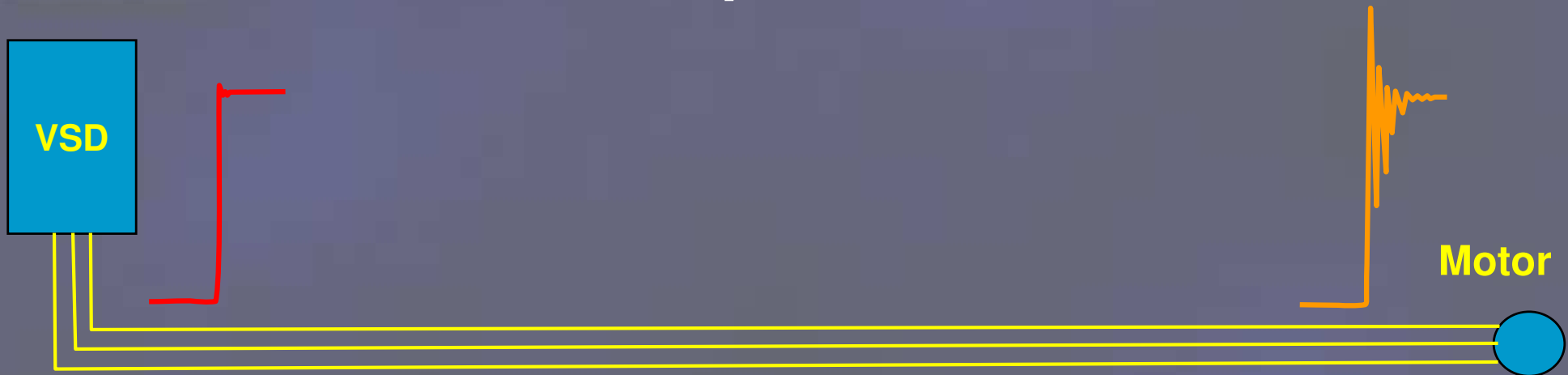
# CAPACITIVE LEAKAGE CURRENTS THE SOLUTION



1. Compensation techniques within the VSD ( This avoids nuisance VSD tripping, but does not necessarily eliminate the capacitive leakage currents )
2. Additional reactance in the VSD output circuit to counter the capacitance, i.e. an output reactor



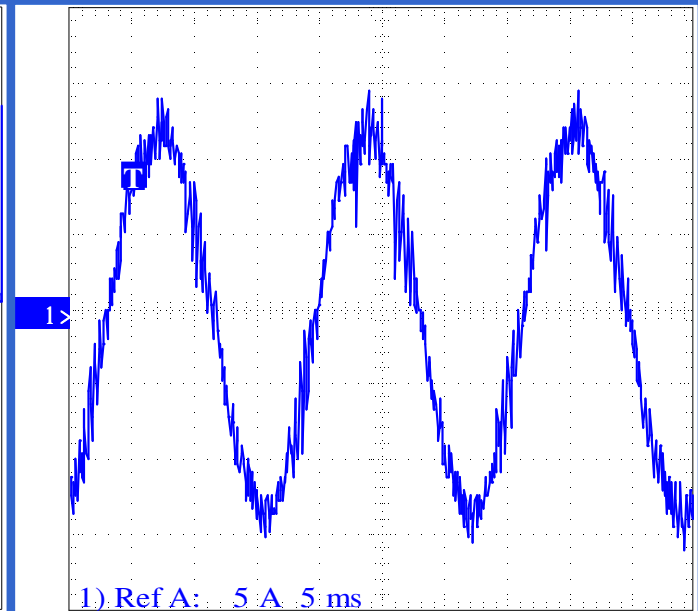
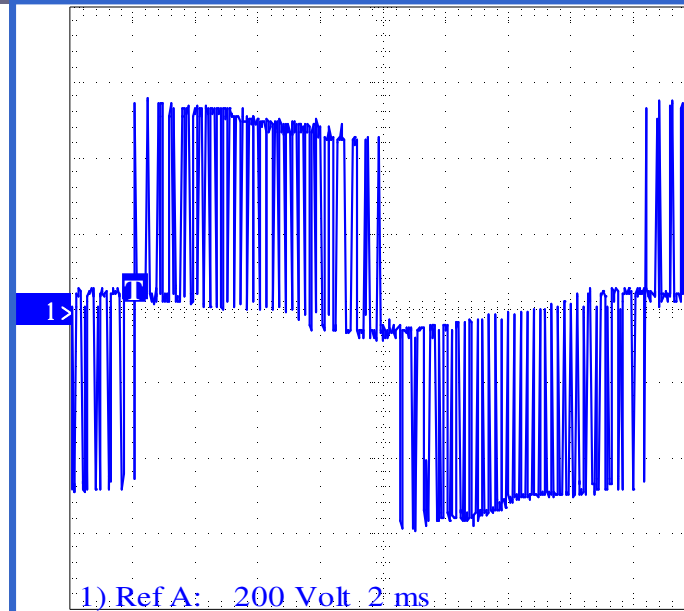
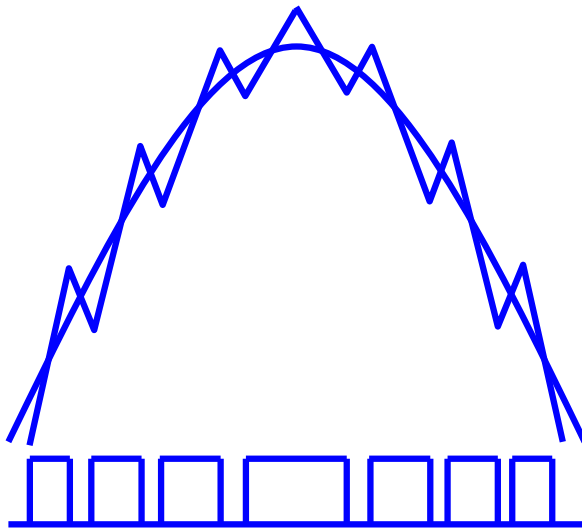
# VOLTAGE REFLECTIONS CAUSING HIGH $V_{peak}$ & $dv/dt$



Voltage pulses from the PWM on the VSD output are reflected at the motor terminals causing voltage pulses significantly higher than the motor nominal voltage



# VOLTAGE REFLECTIONS – THE REALITY

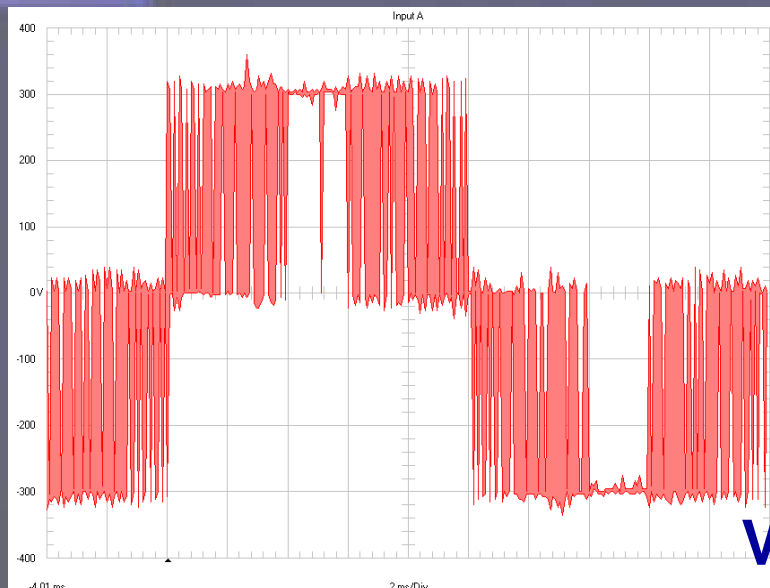


PWM theory

Actual VSD output measurement

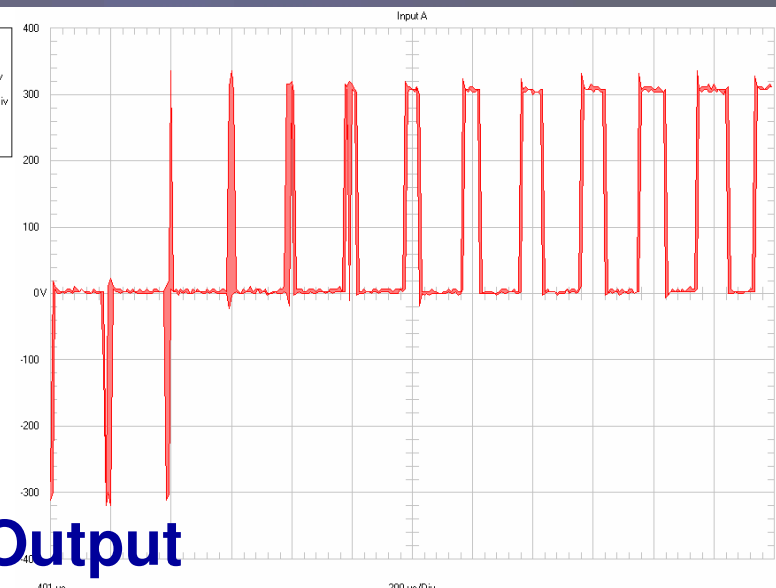


# Voltage reflection measurements

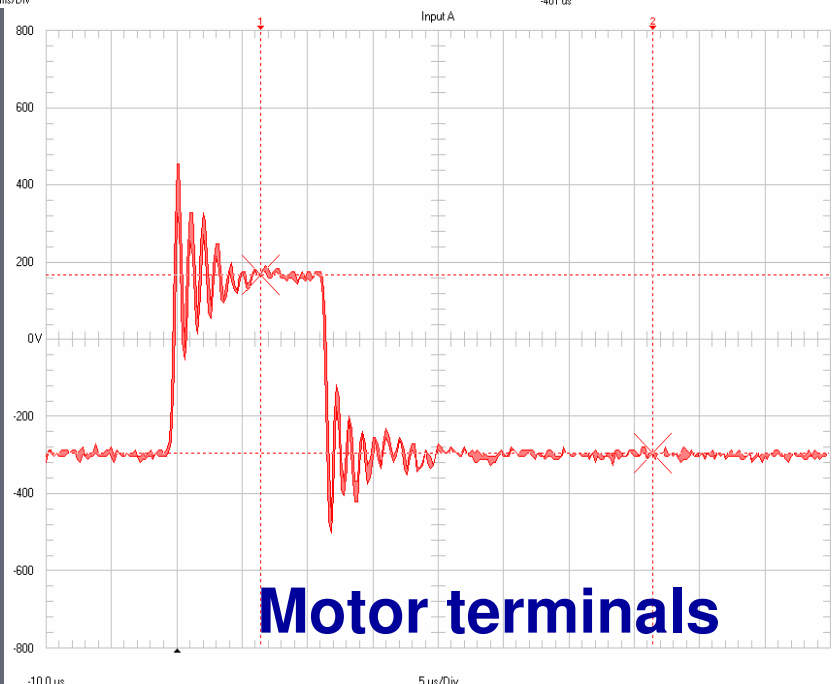


Datablock  
Name = Input A  
Date = 17-Feb-04  
Time = 02:54:43 PM  
Y Scale = 100 V/Div  
Y At 50% = 0 V  
X Scale = 2 ms/Div  
X At 0% = -4.01 ms  
X Size = 300 (300)  
Maximum = 350 V  
Minimum = -336 V

**VSD Output**



Datablock  
Name = Input A  
Date = 17-Feb-04  
Time = 02:57:10 PM  
Y Scale = 100 V/Div  
Y At 50% = 0 V  
X Scale = 200 us/Div  
X At 0% = 401 us  
X Size = 300 (300)  
Maximum = 336 V  
Minimum = -330 V



Datablock  
Name = Input A  
Date = 23-Feb-04  
Time = 08:48:08 AM  
Y Scale = 200 V/Div  
Y At 50% = 0 V  
X Scale = 5 us/Div  
X At 0% = -10.0 us  
X Size = 300 (300)  
Maximum = 456 V  
Minimum = -504 V

Cursor Values  
X1: 6.4 us  
X2: 36.4 us  
dX: 30.0 us  
Y1: 168 168 V  
Y2: -296 -296 V  
dY: -464 -464 V

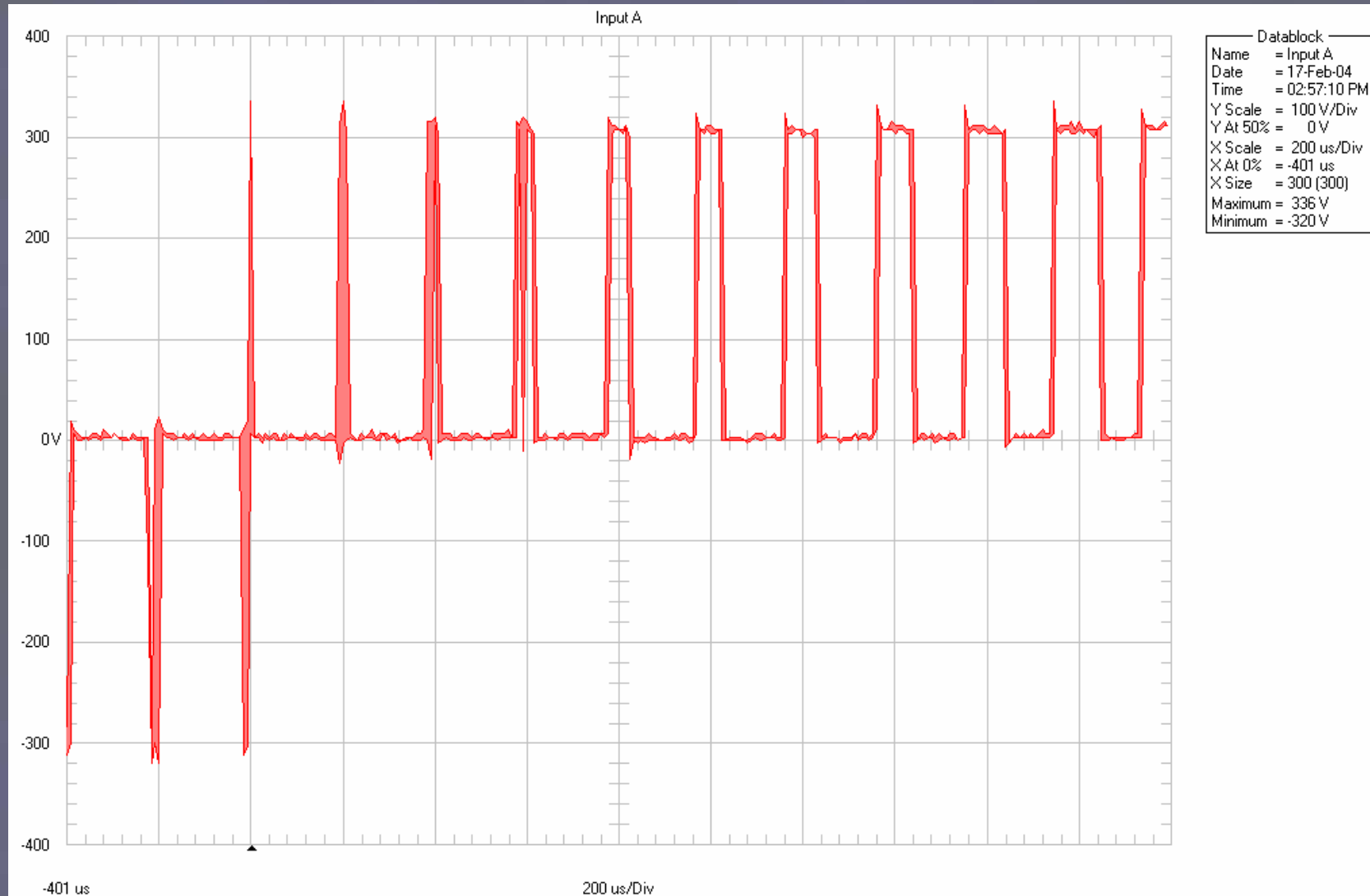
**Motor terminals**







# VOLTAGE REFLECTIONS – Actual measurements

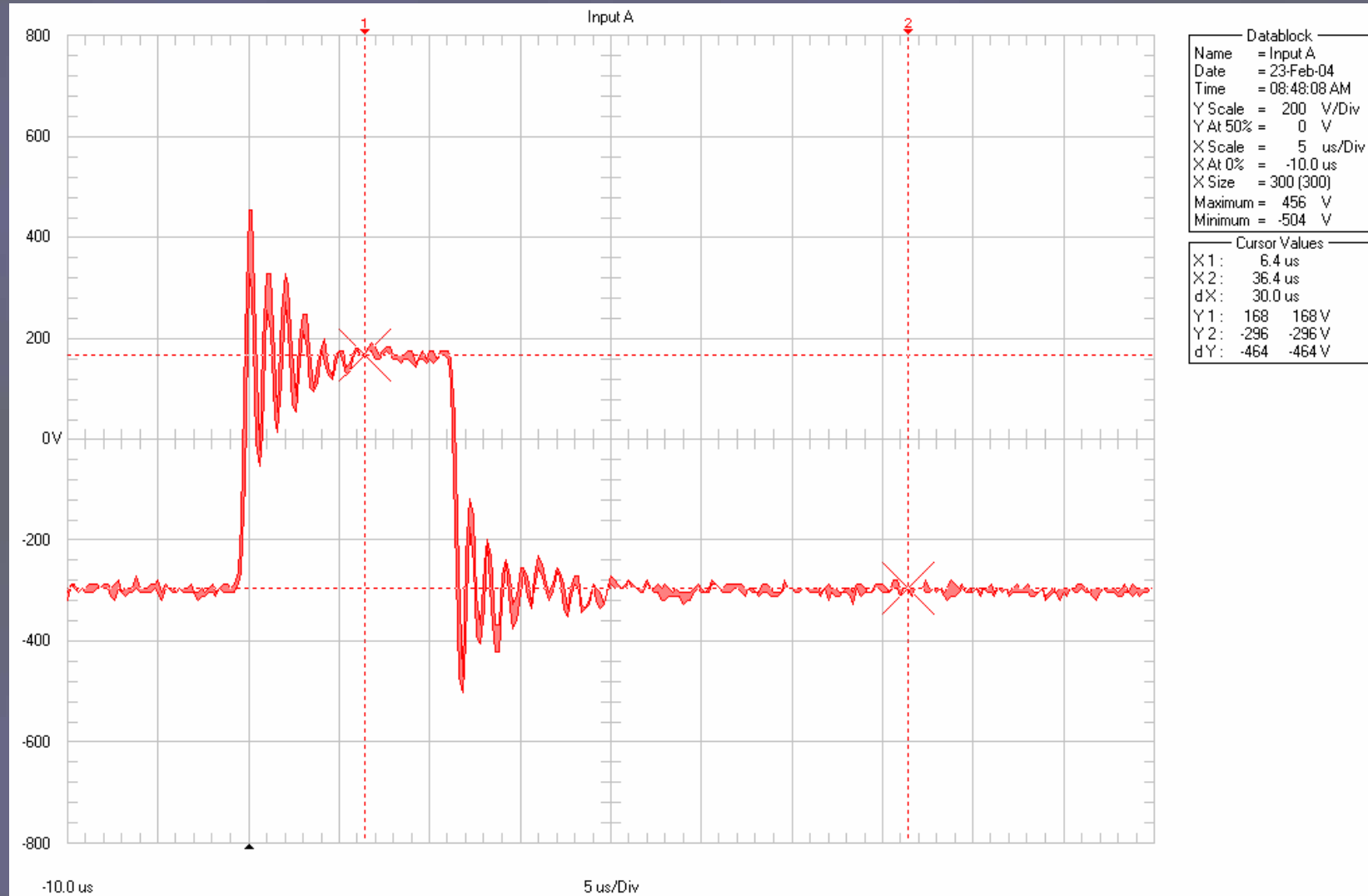


VSD Output





# VOLTAGE REFLECTIONS – Actual measurements



Motor terminals





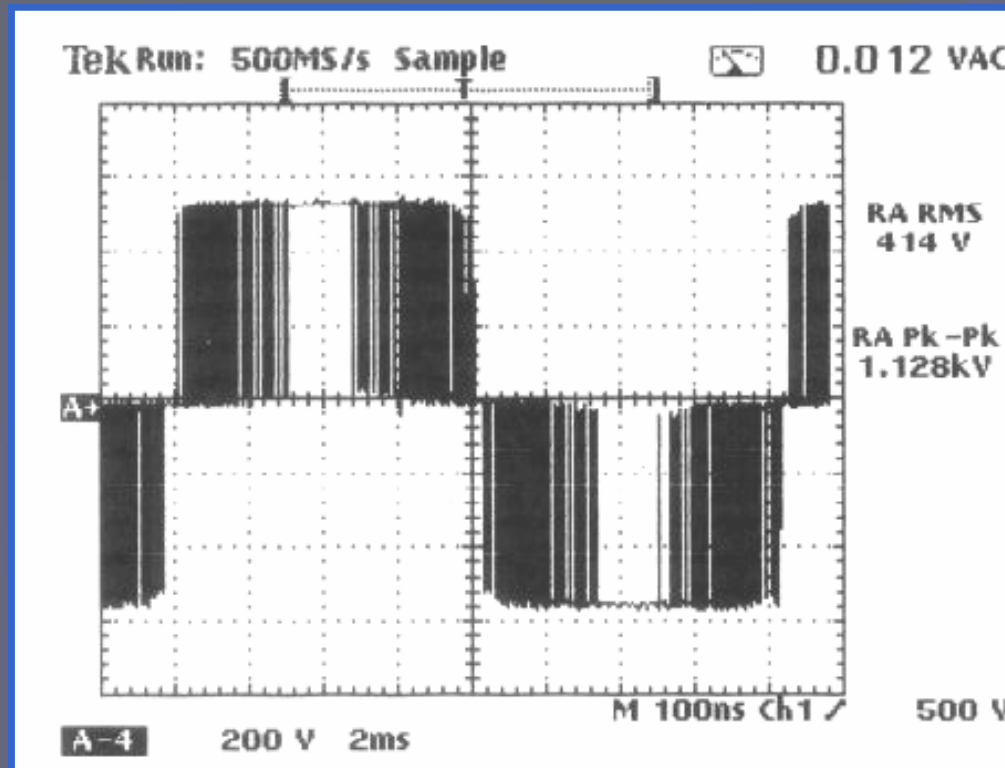
# Influence of the cable length

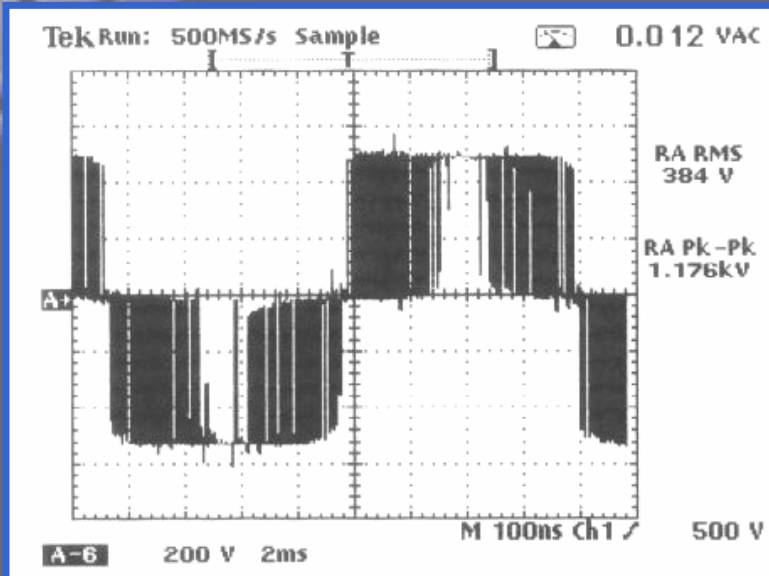
According to NEMA application guide:

- 1.5m cable  $\Rightarrow$  overshoots beginning (overvoltages)
- 15m cable  $\Rightarrow$  may reach 2 times  $V_{DC\ Link}$
- Over 120m  $\Rightarrow$  peaks could be higher than  $2V_{DC\ Link}$  (longer time)

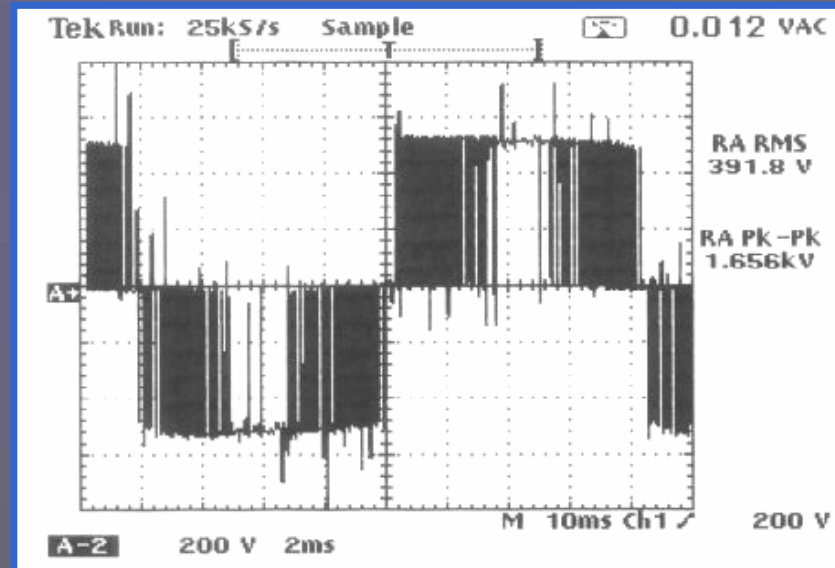
VSD + Standard Motor (7.5kW-380V- IV p)

VSD terminals  
without motor

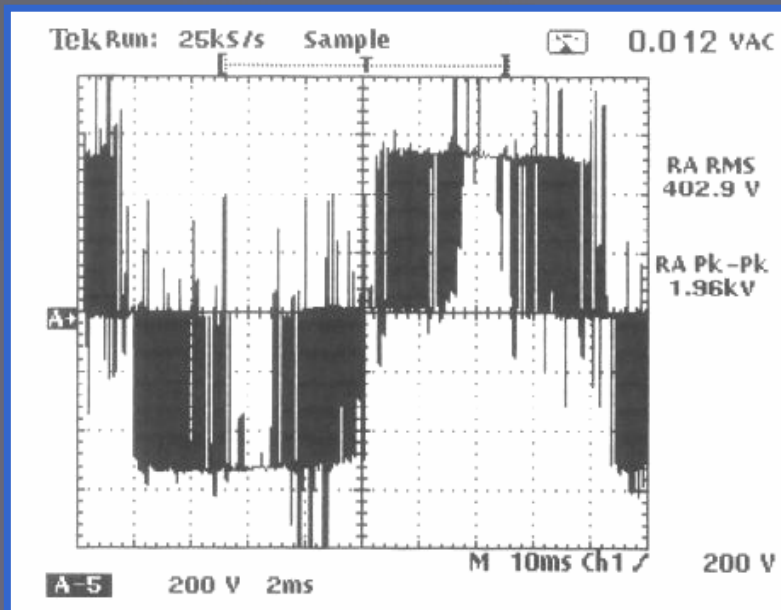




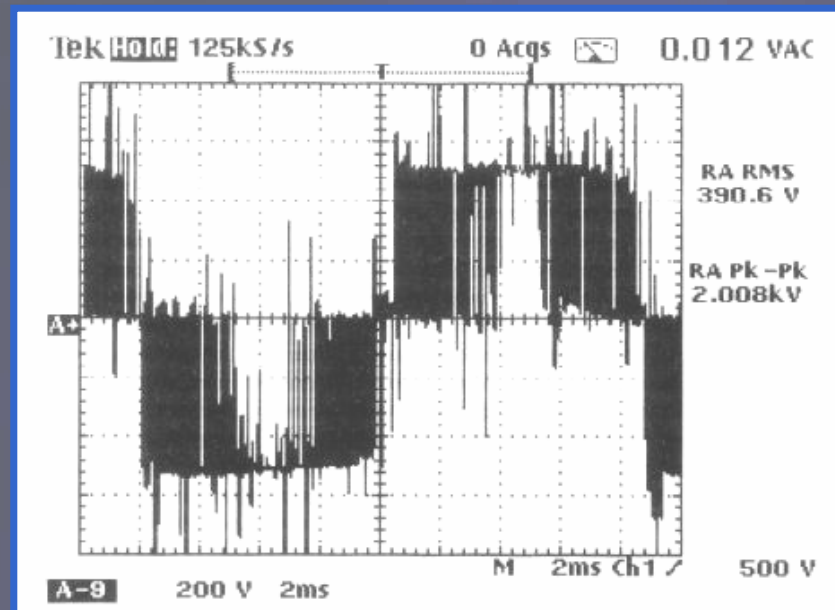
1.5 m cable



15 m cable



34 m cable



54 m cable



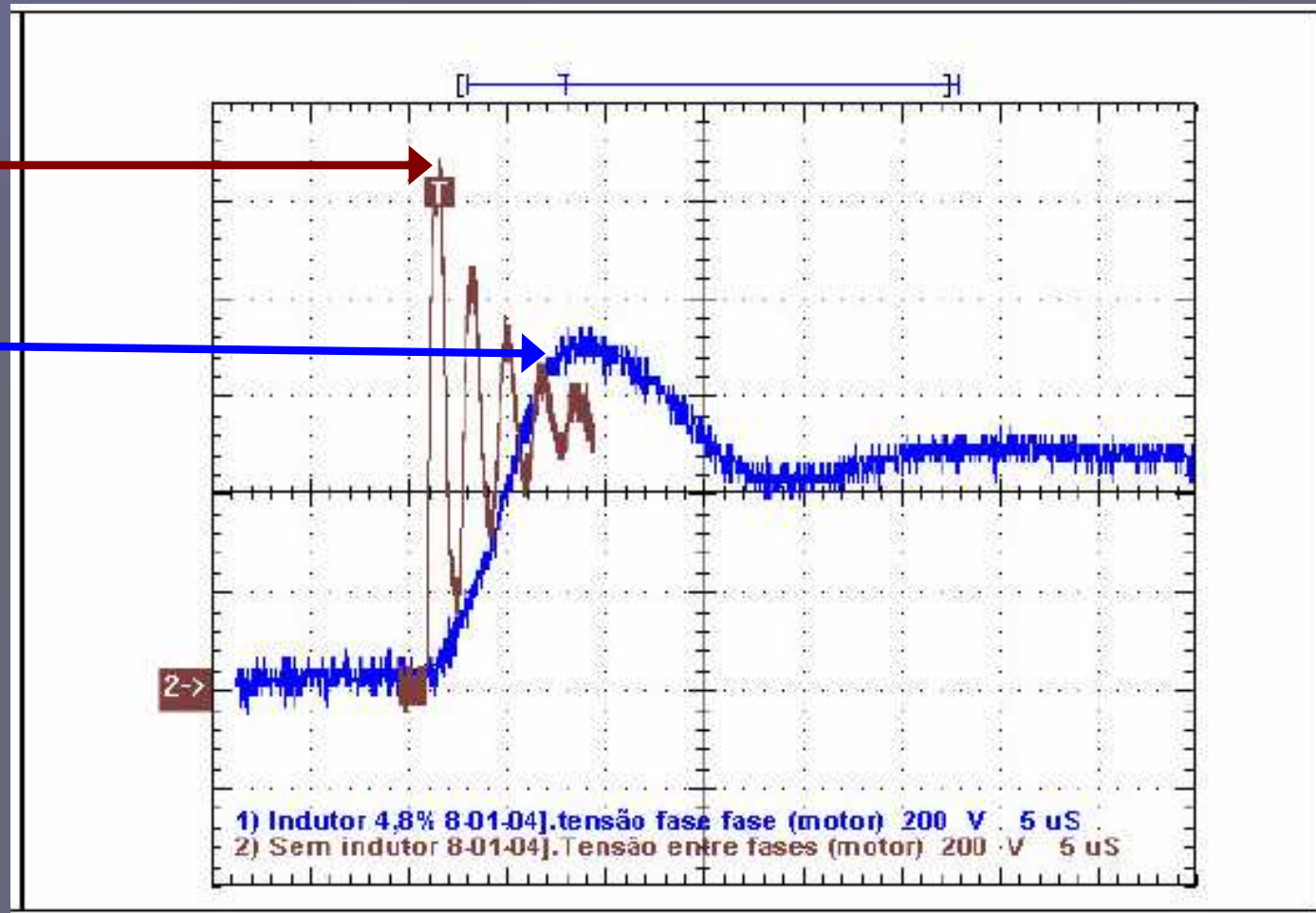


# VOLTAGE REFLECTIONS – Actual measurements

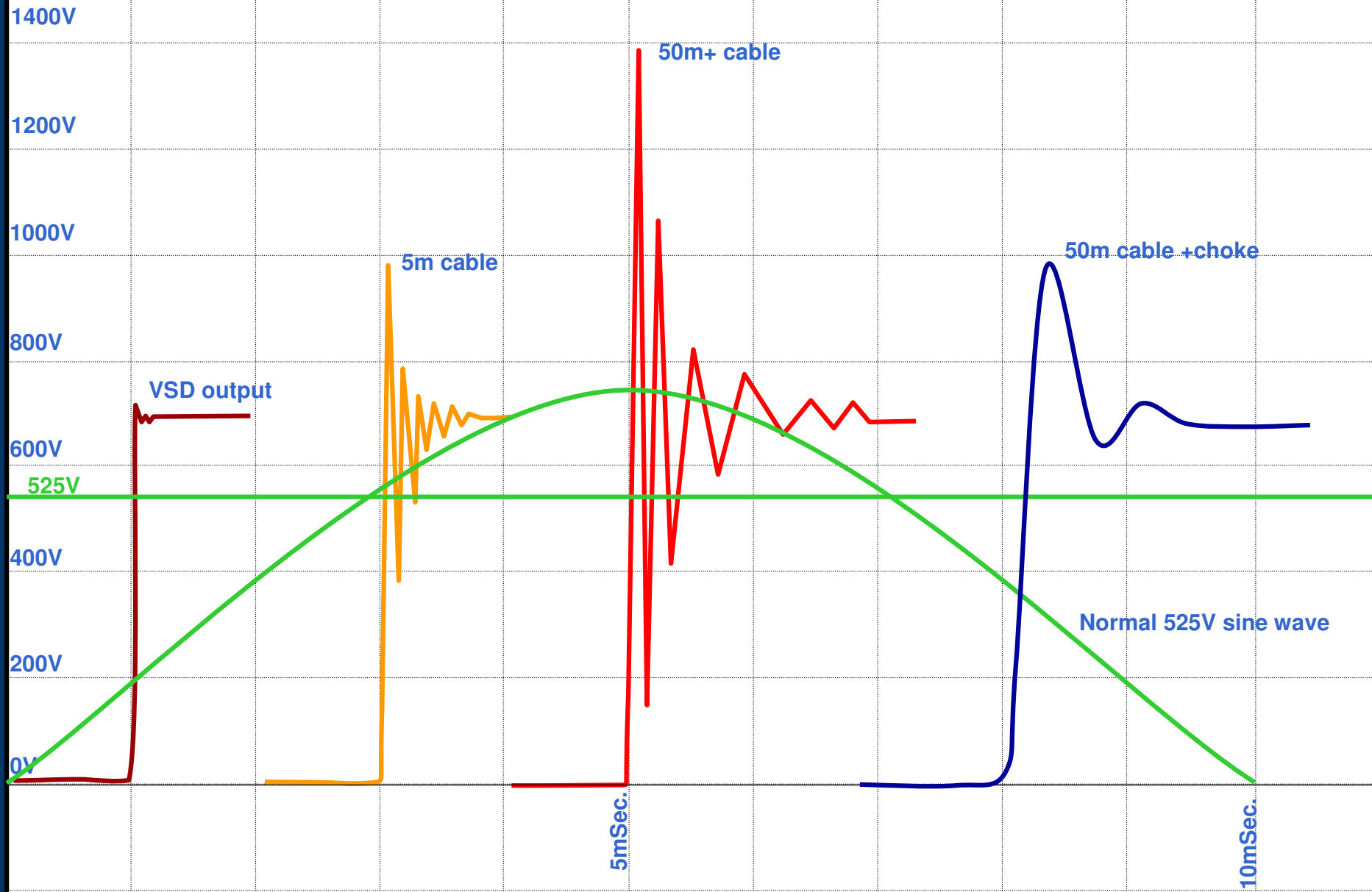
380V supply, 65 m armoured cable, 5.5kW motor & VSD

No reactor  
 $V_p = 975V$   
 $\pm 2.6 \times V_{supply}$

5% reactor  
 $V_p = 667V$   
 $\pm 1.8 \times V_{supply}$



# SUMMARY – VOLTAGE REFLECTIONS AND DV/DT AT MOTOR TERMINALS





# VOLTAGE REFLECTIONS & DV/DT – THE WEG SOLUTION:

1. Design the VSD so that the VSD output  $dv/dt$  is low enough to minimise the  $V_{peak}$  and  $dv/dt$  at the motor terminals
2. Design the motor insulation to withstand  $V_{peak}$  and  $dv/dt$  values in excess of that which the VSD will cause –
  1. Generation 2 wire –  $V_p \leq 1430V$  &  $dv/dt \leq 5200 V/\mu\text{sec}$ .
  2. Generation 3 wire –  $V_p \leq 1780V$  &  $dv/dt \leq 6500 V/\mu\text{sec}$ .
3. Output chokes are always advisable and beneficial to use, but not always mandatory
  1. Counteract capacitive leakage currents
  2. Reduce  $V_{peak}$
  3. Reduce  $dv/dt$
  4. Simple and cost effective to use



**END**